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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,562	04/01/2004	Chih-Hsin Ko	24061.176 (TSMC2003-1247)	1238

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,562	KO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 13-19, and 25-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa et al. (US Pat. No. 5,384,473).

Regarding claims 1 and 27, Yoshikawa et al. teaches a microelectronic device, comprising:

a first semiconductor substrate (10) bonded to a second semiconductor substrate (12) [see fig. 3A], the first semiconductor substrate (10) including an opening (18) [see fig. 3C] through which an epitaxially grown portion (52) of the second semiconductor substrate extends [see fig. 3E];

a first semiconductor device (26) coupled to the first semiconductor substrate (10) [see fig. 3G]; and

a second semiconductor device (28) coupled to the epitaxially grown portion (52) of the second semiconductor substrate [see fig. 3G].

In addition and with regards to claim 27, Yoshikawa et al. teaches the formation of a plurality of openings [col. 2, lines 3-4 and abstract], and a plurality of PMOS and NMOS devices on the corresponding oriented substrates [col. 4, lines 2-6]. Furthermore, Yoshikawa teaches that a dielectric sidewall spacer (50) is included in

each opening (18) [see fig. 3D].

Regarding claims 2, 14 and 28, Yoshikawa et al. further teaches that the first semiconductor device (26) comprises a p-type transistor and the second semiconductor device (28) comprises an n-type transistor [In column 12, lines 60-64, Yoshikawa et al. teaches that it is possible to reverse the surface orientation of the substrate 10 and 12 such that the substrate (10) is formed having a (110) surface orientation and the substrate (12) is formed having a (100) surface orientation. In addition, Yosikawa et al. teaches a preferred embodiment in which NMOS devices (26) are formed on the (100) oriented substrate and PMOS devices (28) are formed on the (110) oriented substrate (Fig. 3G, col. 4, lines 3-9 and 43-47 and col. 5, lines 33-34 -95). Thus, in this embodiment, NMOS devices are formed on the second substrate (12) having the (100) surface orientation and PMOS devices are formed on the first substrate (10) having the (110) surface orientation].

Regarding claims 3, 15 and 29, Yoshikawa et al. teaches that the first semiconductor device (26) comprises an n-type transistor (NMOS) and the second semiconductor device (28) comprises a p-type transistor (PMOS) [col. 5, lines 33-34].

Regarding claims 4, 16 and 30, Yoshikawa et al. further teaches that the first and second semiconductor substrates (10,12) have different crystallographic orientations (110 and 100) [see fig. 3A].

Regarding claims 5, 17 and 31, Yoshikawa et al. further teaches that the first semiconductor substrate (10) has a (1,1,0) crystallographic orientation and the second semiconductor substrate (12) has a (1,0,0) crystallographic orientation [col. 6, lines 60-

64].

Regarding claims 6, 18 and 32, Yoshikawa et al. further teaches that the first semiconductor substrate (10) has a (1,0,0) crystallographic orientation and the second semiconductor substrate (12) has a (1,1,0) crystallographic orientation [see fig. 3A].

Regarding claims 7 and 33, Yoshikawa et al. further teaches a dielectric film (50) interposing a sidewall of the opening (18) and the epitaxially grown portion (52) of the second semiconductor substrate [see fig. 3E].

Regarding claim 13, Yoshikawa et al. further teaches a method of manufacturing a microelectronic device, comprising:

coupling a first semiconductor substrate (10) to a second semiconductor substrate (12) [see fig. 3A];

patterning an opening (18) in the first semiconductor substrate (10) [see fig. 3C];

growing epitaxially an extension of the second semiconductor substrate (52) through the opening (18) [see fig. 3E);

forming a first semiconductor device (26) on the first semiconductor substrate (10) [see fig. 3G]; and

forming a second semiconductor device (28) on the extension of the second semiconductor substrate (52) [see fig. 3G].

Regarding claim 19, Yoshikawa et al. further teaches forming a dielectric film (50) on the first semiconductor substrate (10) opposite the second semiconductor substrate (12) [please note that the sidewall 50 is formed by forming a dielectric film over the substrates 10 and 12. See col. 4, line 68 and col. 5, line 1] and one at least a portion

(50) of a surface of the opening (18) before epitaxially growing the extension of the second semiconductor substrate (52) [see fig. 3D].

Regarding claims 25 and 26, Yoshikawa et al. further teaches that coupling the first semiconductor substrate (10) to the second semiconductor substrate (12) includes bonding the first semiconductor substrate to the second semiconductor substrate [see figs. 3A-3B].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 8-12, 20-24, and 34-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa et al. (US Pat. No. 5,384,473) in view of Furukawa et al. (US Pat. No. 6,555,891 B1).

Regarding claims 8-12, 20-24 and 34, Yoshikawa et al. fails to teach the following limitations:

an oxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the oxide layer;

a silicon dioxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the silicon dioxide layer;

an implanted oxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the implanted oxide layer;

the first semiconductor substrate is a silicon-on-insulator substrate;

a shallow trench isolation interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate, the shallow trench isolation spanning the thickness of the first semiconductor substrate and extending into the second semiconductor substrate; and

planarizing the first semiconductor substrate, the dielectric film, and the extension of the second semiconductor substrate to form a substantially planar surface collectively therefrom, wherein planarizing includes substantially removing all of the dielectric film not located in the opening.

.However and with regards to claims 9-10, 12, 23-24, 35-36 and 38, Furukawa et al. teaches that it is well known in the art to form use a substrate comprising a silicon-

on-insulator (SOI) layer (14) on a bulk semiconductor substrate (12), wherein the SOI layer (14) includes a silicon layer (15) on a silicon oxide layer (16), which is formed on the bulk semiconductor substrate (12) [see fig. 1]. Thus, Furukawa makes obvious the limitation of forming an oxide layer (e.g. silicon dioxide) interposed between the first semiconductor layer and the bulk portion, e.g. to use a SOI substrate.

With regards to the opening, Furukawa further teaches that it is well known in the art to form an opening (10) in the SOI layer, which extends through the oxide layer (16) (see fig. 3).

With regards to the shallow trench isolation as recited in claims 8, 22 and 34, Furukawa teaches a shallow trench isolation (consider the isolation structure 22) interposing a sidewall of the opening (20) and the epitaxially grown portion of the second semiconductor substrate (24) [see fig. 6], the shallow trench isolation (22) spanning the thickness of the first semiconductor substrate (14) and extending into the second semiconductor substrate (12) [see fig. 6].

With regards to the implanted oxide layer as recited in claims 11, 24 and 37, Furukawa further teaches that it is well known in the art to form the oxide layer (16) by implantation of oxygen (col. 3, lines 14-21).

With regards to the planarization step as recited in claims 20-21, Furukawa further teaches that it is well known in the art to planarize the first semiconductor substrate (14), the dielectric film (22), and the extension of the second semiconductor substrate (24) to form a substantially planar surface collectively therefrom and to substantially remove all of the dielectric film (22) not located in the opening (see figs. 5-

6 and col. 5, lines 2-5).

Yoshikawa et al. and Furukawa are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include the limitations of: an oxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the oxide layer; a silicon dioxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the silicon dioxide layer; an implanted oxide layer interposing the first semiconductor substrate and a bulk portion of the second semiconductor substrate, the opening also extending through the implanted oxide layer; the first semiconductor substrate is a silicon-on-insulator substrate; and planarizing the first semiconductor substrate, the dielectric film, and the extension of the second semiconductor substrate to form a substantially planar surface collectively therefrom, wherein planarizing includes substantially removing all of the dielectric film not located in the opening; and to form a shallow trench isolation interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate, the shallow trench isolation spanning the thickness of the first semiconductor substrate and extending into the second semiconductor substrate.

The motivation for doing so is to reduce leakage current and parasitic capacity. Therefore, it would have been obvious to combine Furukawa with Yoshikawa et al. to obtain the invention of claims 8-12, 20-24, and 34-38.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/28/05

José R. Díaz
Examiner
Art Unit 2815